Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

Kindly cancel claims 1-29 and substitute the following new claims therefore:

1-29 (cancelled)

30. (Currently amended) Apparatus comprising:

a plurality of adaptive computing elements connected in a ring configuration, including

a plurality of processing elements connected in a chain configuration and including a first processing element at a first end of the chain and a second processing element at a second end of the chain, and

a control element connected to the first processing element and the second processing element, and operative to manage data entering the ring;

a bus; and

an interface device connected between the control element and the bus, wherein each of the adaptive computing elements comprises a Field Programmable Gate Array integrated circuit, and wherein the ring includes two processing elements.

31. (cancelled)

32. (cancelled)

33. (cancelled)

34. (Original) The apparatus of claim 30, wherein the bus comprises a PCI (Peripheral Component Interconnect) bus.

35. (Original) The apparatus of claim 30, wherein the bus comprises a VME (Versa Module Europa) bus.

36. (Original) The apparatus of claim 30, further comprising a host processor connected to the bus and operative to configure the adaptive computing elements.

37. (Original) The apparatus of claim 30, wherein the apparatus comprises an adaptive computing system (ACS) accelerator.

38. (Original) The apparatus of claim 30, further comprising a memory device connected to each of the processing elements.

39. (Original) The apparatus of claim 38, wherein each memory device comprises an SRAM (Static Random Access Memory).

40. (Original) The apparatus of claim 30, wherein the interface device is integrated in the control element.

41. (Original) The apparatus of claim 30, further comprising an integrated circuit including the processing elements and the control element.

42. (Original) The apparatus of claim 30, wherein the interfaces device comprises an FPGA (Field Programmable Gate Array) integrated circuit.

43. (Currently amended) ~~The apparatus of claim 30,~~ An Apparatus comprising:

a plurality of adaptive computing elements connected in a ring configuration, including

a plurality of processing elements connected in a chain configuration and including a first processing element at a first end of the chain and a second processing element at a second end of the chain; and

a control element connected to the first processing element and the second processing element, and operative to manage data entering the ring;

a bus;

an interface device connected between the control element and the bus;

a second plurality of adaptive computing elements connected in a second ring configuration, including

a plurality of processing elements connected in a chain configuration and including a third processing element at a first end of the chain and a fourth processing element at a second end of the chain, and

a control element connected to the first processing element and the second processing element, and operative to manage data entering the ring;

a first data path connected the first processing element and the fourth processing element; and

a second data path connected between the second processing element and the third processing element.

44. (New) An apparatus, comprising:

a first system comprising:

a plurality of nodes, connected together, each node including reconfigurable logic, which can be reconfigured according to a command;

an interface circuit, including a plurality of buffers, capable of sending and receiving data;

a host program, which enables configuring a plurality of different objects, including :

a remote node object, which produces said command to configure a node that is on a system that is remote from a said first system;

a local node object, which produces said command to configure a node that is on a system that is local to said first system; and

a channel object, which configures a channel between said interface circuit on said first system, and a second interface circuit on a second system, to allow data to be passed between configured nodes on the first system and configured nodes on the second system, via said channel object.

45. An apparatus as in claim 44, wherein said plurality of nodes are connected together in a ring structure.

46. (New) An apparatus as in claim 45, wherein one of the nodes in the ring is configured as a controlling node, and passes data between the interface circuit and the other nodes of the ring.

47. (New) An apparatus as in claim 44, wherein said interface circuit includes a plurality of addressable FIFO buffers, and said channel object configures a channel between a FIFO buffer on said first system and a FIFO buffer on said second system.

48. (New) An apparatus, comprising:

a first system comprising:

a plurality of nodes, connected together, each node including reconfigurable logic, which can be reconfigured according to a command;

an interface circuit, including a plurality of buffers, capable of sending and receiving data to other interface circuits of other systems;

a host program, which enables configuring a plurality of different objects, including :

a remote node object, which produces said command to configure a node that is on a system that is remote from said first system;

a local node object, which produces said command to configure one of said nodes that is on a system that is local to said first system; and

a channel object, which configures a channel between said interface circuit on said first system, and another interface circuit, to allow data to be passed between configured nodes on the first system and configured nodes on the second system, via said channel object; and

a second system, comprising:

a plurality of nodes, connected together, each node including reconfigurable logic, which can be reconfigured according to a command;

an interface circuit, including a plurality of buffers, capable of sending and receiving data to said interface circuit on said first system;

a host program, which enables configuring a plurality of different objects, including :

a remote node object, which produces said command to configure a node that is on said first system;

a local node object, which produces said command to configure a node that is on a system that is local to said second system; and

a channel object, which configures a channel between said interface circuit on said first system, and said interface circuit on said second system, to allow data to be passed between configured nodes on the first system and configured nodes on said second system, via said channel object.